2. RELATED APPEALS AND INTERFERENCES

There are no interferences or appeals known to the Appellant, Appellant's legal representative, or the assignee that will directly affect or be directly affected by or have a bearing on the Board's decision in an appeal.

3. STATUS OF THE CLAIMS

Claims 26-49 are currently pending and are appealed. No claims have been canceled or added. The pending claims are listed in Appendix I.

4. STATUS OF AMENDMENTS

No amendments were made subsequent to the final Office Action dated April 25, 2002.

5. SUMMARY OF THE INVENTION

As described in the Appellant's specification at page 6, line 3 - page 7, line 3, and shown generally in figures 1-5, embodiments of the invention disclosed relate to a memory device that can operate in either burst or extended data out (EDO) modes of operation, while maintaining a standard dynamic random access memory pinout. In one embodiment, the device is organized as a 2 Meg x 8 burst EDO dynamic random access memory (DRAM) having a standard EDO RAM pinout. Pg. 10, lines 18-23. Row address strobe signals and column address strobe (CAS/) signals can be used to latch the first and second portions of an address, respectively. Pg. 10, line 23 - Pg. 11, line 6. During a burst read operation, the CAS/ signal may be used to advance the address from which data is obtained. Pg. 11, lines 10-23. During a burst write operation, the CAS/ signal may be used to latch data at the inputs. Pg. 15, lines 4-12. A signal, such as the write enable (WE/) signal, may be used to select the operational mode of the memory. (Pg. 16, lines 1-3). The memory can be accessed in a linear or interleaved fashion. Pg. 12, lines 9-10. In addition to the embodiment described, the invention includes other embodiments of varying scope, including systems, methods, and storage devices, such as memory circuits. (FIGs. 6-11; and Pg. 25, line 1 - Pg. 39, line 7).

6. ISSUES PRESENTED FOR REVIEW

1. Whether claims 26, 29, 32, 35-39, and 40 were properly rejected under 35 USC § 102(a) as being anticipated by "Intel" Electronic News, December 5, 1994 (hereinafter "EN") in view of 82430FX PCIset DATASHEET 82437FX System CONTROLLER (TSC) AND 82438FX DATA PATH UNIT (TDP), Intel Corp., pp 1-67, 11/96 (hereinafter "Intel").

2. Whether claims 27-28, 30-31, 33, 34, and 41-49 were properly rejected under 35 USC § 103(a) as being unpatentable over EN in view of Intel, and further in view of Fung et al. (U.S. Patent Number 5,630,163, hereinafter "Fung").

3. Whether claims 26, 29, 32, and 35-39 were rejected under 35 USC § 103(a) as being unpatentable over Farrer et al. (U.S. Patent Number 5,307,320, hereinafter "Farrer") in view of "Reduce DRAM Cycle Times With Extended Data-Out", Micron technical Note pp. 5-33 thru 5-40, 4/94 (hereinafter "Micron"), and further in view of Wyland (U.S. Patent Number 5,261,064, hereinafter "Wyland").

4. Whether claims 27-28, 30-31, 33, 34, and 41-49 were properly rejected under 35 USC § 103(a) as being unpatentable over Farrer in view of Micron, and further in view of Wyland and Fung.

7. GROUPING OF THE CLAIMS

All claims are to be taken independent of each other and each stands alone for purposes of this appeal.

8. ARGUMENT

a) The Applicable Law

Anticipation requires the disclosure in a single prior art reference of each element of the

claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim*." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131.

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d (BNA) 1596, 1598 (Fed. Cir. 1988). In combining prior art references to construct a *prima facie* case, the Examiner must show some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art that would lead an individual to combine the relevant teaching of the references. *Id.* The M.P.E.P. contains explicit direction to the Examiner that agrees with the *In re Fine* court:

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d (BNA) 1438 (Fed. Cir. 1991)).

An invention can be obvious even though the suggestion to combine prior art teachings is not found in a specific reference. *In re Oetiker*, 977 F.2d 1443, 24 U.S.P.Q.2d (BNA) 1443 (Fed. Cir. 1992). However, while it is not necessary that the cited references or prior art specifically

suggest making the combination, there must be some teaching somewhere which provides the suggestion or motivation to combine prior art teachings and applies that combination to solve the same or similar problem which the claimed invention addresses. One of ordinary skill in the art will be presumed to know of any such teaching. (See, e.g., *In re Nilssen*, 851 F.2d 1401, 1403, 7 U.S.P.Q.2d 1500, 1502 (Fed. Cir. 1988) and *In re Wood*, 599 F.2d 1032, 1037, 202 U.S.P.Q. 171, 174 (C.C.P.A. 1979)). However, the level of skill is not that of the person who is an innovator but rather that of the person who follows the conventional wisdom in the art. *Standard Oil Co. v. American Cyanamid Co.,* 774 F.2d 448, 474, 227 U.S.P.Q. 293, 298 (Fed. Cir. 1985). The requirement of a suggestion or motivation to combine references in a *prima facie* case of obviousness is emphasized in the Federal Circuit opinion, *In re Sang Su Lee*, 277 F.3d 1338; 61 U.S.P.Q.2D 1430 (Fed. Cir. 2002), which indicates that the motivation must be supported by evidence in the record.

The test for obviousness under § 103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 U.S.P.Q. 543, 551 (Fed. Cir. 1985). The Examiner can only rely on references which are either in the same field as that of the invention, or if not in the same field, the references must be "reasonably pertinent to the particular problem with which the inventor was concerned." *M.P.E.P.* § 2141.01 (a) (citing *In re Oetiker*, 24 U.S.P.Q.2d (BNA) 1443 at 1445). The Examiner must also recognize and consider not only the similarities but also the critical differences between the claimed invention and the prior art. *In re Bond*, 910 F.2d 831, 834, 15 U.S.P.Q.2d (BNA) 1566, 1568 (Fed. Cir. 1990), *reh'g denied*, 1990 U.S. App. LEXIS 19971 (Fed. Cir. 1990).

If the proposed modification renders the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *M.P.E.P.* § 2143.01 (citing *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984)). The Examiner must also avoid hindsight. *Id.* The Examiner cannot use the Appellant's structure as a "template" and simply select elements from the references to reconstruct the claimed invention. *In re Gorman,* 933 F.2d 982, 987, 18 U.S.P.Q.2d (BNA)

1885, 1888 (Fed. Cir. 1991).

b) The References

EN: discloses the existence of the Triton (82430FX) Peripheral Component Interconnect (PCI) chipset which has the capability to support main memory using EDO and standard page mode memory DRAMs, as well as a cache using burst, pipelined burst, or standard static random access memories (SRAMs). (Pg. 2, paras. 1-5). Use of an interchangeable mode memory device, or burst extended data out memory, is not disclosed.

Intel: describes the 82430FX Host-to-PCI bridge chip set with cache control and a data path to main memory. (Pg. 6, Col. 1, paras. 1-2). Main memory can use standard page mode and EDO RAM memory between rows. (Pg. 31, 3.2.16). The memory type may be detected using a Basic Input/Output System (BIOS) algorithm. (Pg. 45, Col. 1, paras. 2-3). Asynchronous, synchronous burst, and pipelined burst SRAMs may be used for cache memory. (Pg. 34, Col. 2, para. 3). Use of an interchangeable mode memory device, or burst extended data out memory, is not disclosed.

Fung: describes a data processing system having processor, a bus, RAM, and Read Only Memory (ROM). (Col. 3, lines 47-65). The existence of a BIOS having self-test routines is included. (Col. 1, lines 25-33). The content of the self-test routines is not discussed.

Farrer: teaches a memory controller which is programmable to operate with different types of DRAMs. (Col. 5, lines 58-62). Timing parameters can be selected using registers. (Col. 6, lines 2-13). Operating with EDO and/or burst mode memories is not described.

Micron: describes the differences between fast page mode memory and EDO memory. (Pg. 5-34, Cols. 1-2). The article goes on to show how, in some cases, EDO memory may be substituted for fast page memory. (Pg. 5-33, Col. 2). Explicit cases where EDO memory can not be used in this manner are also described. (Pg. 5-39, Col. 2). Operations using memory devices capable of burst operation, or interchangeable EDO and burst operation, are not discussed.

Wyland: teaches a dual-port DRAM that can be operated in burst mode. (Col. 2, lines 3-5). Access in a random fashion is also permitted. (Col. 3, lines 9-13). EDO operation is not disclosed.

c) Discussion of the Rejections

c.1 The rejection under § 102:

Claims 26, 29, 32, 35-39, and 40 were rejected under 35 USC § 102(a) as being anticipated by EN in view of Intel. First, the Appellant does not admit that EN or Intel are prior art and reserves the right to swear behind these references in the future. Second, the Appellant respectfully submits that a case of anticipation under 35 U.S.C. § 102(a) has not been made because EN and Intel do not disclose each and every element of claims 26, 29, 32, 35-39, and 40. Therefore, the Appellant respectfully traverses this rejection under 35 U.S.C. § 102(a).

Why the reference does not disclose each and every element of the claimed subject matter as arranged in the claims.

EN specifically does not disclose "a memory device which is interchangeably of a mode selected from the group consisting of burst extended data out mode and fast page mode" as claimed by the Appellant in claim 26, or "a memory device which is interchangeably of a mode selected from the group consisting of burst extended data out mode and extended data out mode" as claimed in claim 29. EN also does not disclose "a memory device operable in a mode selected from the group consisting of burst extended data out mode and a second operation mode" as claimed in claims 32 and 40, "a first bank of burst extended data out memory" as claimed in claims 35, 36, and 38, or "a first bank and a second bank, wherein the first bank and the second bank are each independently interchangeably of a memory type selected from the group consisting of burst extended data out memory and a second type of memory" as claimed in claims 37 and 39.

As noted above, EN merely teaches the alternative use of EDO and page mode RAMs in main memory. See EN, Pg. 2, para. 5. EDO burst mode operations are not discussed.

Intel also does not disclose these elements since operations using burst EDO memories are not discussed. As noted above, Intel merely teaches the use of standard page mode and EDO

RAM in main memory. See Intel, Pg. 41, Col. 2, para. 4. While it is asserted in the Office Action that FIG. 1 and pgs. 1, 24, 31, and 41-45 of Intel disclose burst operation, the Appellants' representative was only able to find references to synchronous burst and pipelined burst SRAMS, and not burst EDO memories. (Pg. 34, Col. 2, para. 3).

The use of devices operable in burst EDO *and* another mode (claims 26, 29, 32, and 40), or using burst EDO memory in one bank and a different type of memory in a second bank (claims 35-39) are not disclosed in this reference. Thus, the assertion that "These inherent features are disclosed by Intel ..." is incorrect.

The reference "P55TP4 (Triton-Based) SYNC/BURST SRAMS?" (an email exchange between unknown parties on the internet) is again offered as a reference in the Office Action to show that the "Triton chipset board can mix and max [sic] with normal fast page mode and EDO memory". However, the relative authority of this reference, as well as the level of skill of the contributors is doubtful, since some of the contributors declare themselves right, and the others wrong. Further, all of the statements made by the contributors are based on hearsay. Still further, the reference is non-enabling. Finally, this reference adds nothing to Intel, previously discussed. Therefore it is respectfully submitted that this reference is irrelevant to the matter at hand.

Why the reference does not disclose the claimed subject matter in as complete detail as is contained in the claim.

A case of anticipation has not been established. While the assertion is made that both EN and Intel disclose the invention as claimed, the Appellant's representative was unable to locate any discussion, or circuitry, directed to burst EDO memory operations, as claimed in claims 26, 29, 32, and 35-40..

The only references offered by the Office to support the assertion are from Intel: FIG.1, and pages 1, 24, 31, and 41-45. However, these pages merely discuss the use of EDO and standard page mode DRAMs. See, for example, Intel, Col. 1, para. 2. Thus, Intel never discusses the ability to operate using a controller and a combination of burst EDO and other types of memory devices, or addressing a memory device which is operable between the these two modes, as claimed by the Appellant in independent claims 26, 29, 32, and 35-40. And, as noted

previously, the mere presence of a computer system does not imply the use of different memory types; the selection of memories is left up to the designer and/or purchaser of a system.

In short, what is discussed by EN and Intel is not identical to the subject matter of the present invention as required by the M.P.E.P., and therefore, the rejection under § 102 is improper. Reconsideration and allowance of claims 26, 29, 32, and 35-40 is respectfully requested.

c.2 The rejections under § 103:

Claims 27-28, 30-31, 33, 34, and 41-49 were rejected under 35 USC § 103(a) as being unpatentable over EN in view of Intel, and further in view of Fung. Claims 26, 29, 32, and 35-39 were rejected under 35 USC § 103(a) as being unpatentable over Farrer in view of Micron, and further in view of Wyland. Claims 27-28, 30-31, 33, 34, and 41-49 were rejected under 35 USC § 103(a) as being unpatentable over Farrer in view of Micron, and further in view of Wyland and Fung.

First, the Appellant does not admit that EN, Intel, Fung, Farrer, Micron, or Wyland are prior art and reserves the right to swear behind these references in the future. Second, because the systems taught in the references are not the same as that claimed by the Appellant, and can not be combined to operate as such, and further, since each of the references do not teach the element of a burst EDO memory operation (or the use of a device operable in burst EDO *and* other modes), and finally, since Fung, Farrer, Wyland, and Micron teach away from any such combination, the Appellant respectfully traverses this rejection under § 103 by the Office.

The Appellant's representative is unable to find how EN, Intel, and Fung, in combination with each other, serve to teach the invention disclosed in claims 27-28, 30-31, 33, 34, and 41-49. The Appellant has already discussed the deficiencies of EN and Intel as references. And, as admitted in the Office action "... neither EN nor Intel specifically discloses a power supply; and a power up detection circuit ... to cause the processor to detect the memory device mode ...".

In the Office Action, Fung is alleged to provide a "power up detection circuit coupled to the processor and the power supply", because a "BIOS reads on this limitation since the BIOS operates during a power up routine". However, since a BIOS is merely a collection of software routines, no power up detection circuitry is necessarily involved, much less connected and

operable as claimed by the Appellant. In fact, nowhere in Fung is a power up detection circuit shown or described. Thus, combining Fung with the EN and Intel references produces a system which is inoperative to detect the mode of the memory devices responsive to a power up detection circuit.

Therefore, the Office Action assertion that Fung discloses a "power up detection circuit" is erroneous, and it is respectfully submitted that a *prima facie* case of obviousness has not been established at least because the cited references do not teach or suggest "a power up detection circuit", as recited in claims 27-28, 30-31, 33, 34, and 41-49. Further, the Intel reference is predated by the instant Application priority filing date, and it is thus improper to combine Intel with the EN reference under 35 USC § 103(a). As noted by the CCPA, "... the inherency of an advantage and its obviousness are entirely different questions. That which may be inherent is not necessarily known. Obviousness cannot be predicated on what is unknown." See *In Re Sportmann*, 150 USPQ 449 (C.C.P.A. 1966). For these reasons, claims 27-28, 30-31, 33-34, and 41-49 should be in condition for allowance, due to the combined deficiencies of Fung and Intel.

Claims 26, 29, 32 and 35-39 were rejected under 35 USC § 103(a) as being anticipated by Farrer in view of Micron, and further in view of Wyland. However, it is admitted in the Office Action that Farrer does not disclose a memory including EDO and fast page mode elements, and that neither Farrer nor Micron disclose burst mode operations, as claimed by the Appellant.

It is asserted in the Office Action that Micron can be combined with Farrer to supply these missing elements to provide a system which detects memory modes and then programs the memory controller accordingly. The Appellant respectfully notes that neither Farrer, Micron, nor Wyland provide a processor which responds to information (including data read from the memory device) to program the memory controller for the provision of memory access signals, as claimed by the Appellant in claims 26, 29, 32, and 38-39. Further, none of these references teach the use of individual memory devices which operate in burst EDO *and* another mode, as claimed by the Appellant in claims 26, 29, and 32.

Further, neither Farrer, Micron, nor Wyland teach a memory controller operating interchangeably with banks of burst EDO memory and other memories, as claimed by the Appellant in claims 35-37. It is respectfully noted that Micron does not teach interchangeable

memories, as asserted in the Office Action. Rather, Micron demonstrates that given the proper circumstances, regular (non-burst) EDO memory may sometimes be substituted for standard fast page mode memory. In fact, Micron notes that there are specific cases where EDO substitution is *not* possible. (Pg. 5-39, Col. 2). Thus, memory systems designed for EDO memory will *not* necessarily allow the substituted use of standard fast page mode memory, and there is no teaching in Micron to combine the use of burst EDO memory and another type of memory between banks, as claimed by the Appellant in claims 35-39.

Claims 27-28, 30-31, 33-34, and 41-49 were rejected under 35 USC § 103(a) as being anticipated by Farrer and Micron, in view of Wyland and Fung. As noted above, the admitted defect of Farrer, Wyland, and Micron to teach a power-up detection circuit of the type claimed by the Appellant can not be remedied by Fung, which merely discloses the operation of a BIOS. Fung does not mention a power up detection circuit, or responsively detecting memory device modes of operation. Thus, combining Fung with Ferrer, Wyland, and Micron provides a system which is inoperative to detect memory device types in response to power up detection circuit activity.

Further, Farrer, Micron, Wyland, and Fung can not be combined to demonstrate the use of burst EDO memory in combination with the other claimed elements of the invention. Pursuant to MPEP § 2144.03, the Appellant requests that one or more specific references supporting this particular combination to be provided. In the absence of such references, the Appellant asserts the burden of establishing a *prima facie* case of obviousness has not been met, and requests reconsideration and withdrawal of the rejection of claims 27-28, 30-31, 33-34, and 41-49 under 35 USC § 103(a).

It is also respectfully noted that there is no evidence in the record to support combining the references, as required by *In Re Sang Su Lee*. While assertions are made in the Office Action that it would be "obvious ... to include ... a power up detection circuit coupled to the processor and power supply to cause the processor to detect the memory device mode ... to program the memory controller ... for the advantages stated above", or "obvious ... to include ...a memory device which is interchangeably of a mode selected from ... EDO mode and fast page mode ... for the advantages stated above", or "obvious ... to use burst access memory of Wyland in the

combined invention of Farrer and Wyland for the purpose of increasing [sic] access time", nothing other than the knowledge of the Examiner is in evidence. The complete absence of evidence in the record to support a combination of the references does not satisfy the explicit requirements set forth by the *In re Sang Su Lee* court. Thus, it is respectfully requested that the Examiner submit an affidavit as required by 37 C.F.R. § 1.104(d)(2) to sustain this use of personal knowledge.

Further, it is improper to combine Micron with the other references. Micron teaches substitution of memory devices under limited circumstances, and describes specific situations where substitution will in fact fail to produce an operative system. The M.P.E.P. requires that the asserted combination of the references must not render the prior art unsatisfactory for its intended purpose, or change the principle of operation of the reference being modified. *See* M.P.E.P. § 2143.01. One of ordinary skill in the art would not be led to use memory in an interchangeable fashion, given the expectation of failure noted by Micron (as opposed to the reasonable expectation of success required for a *prima facie* case to be established according to the M.P.E.P. and the *In Re Fine* court). It is also improper to combine references where the references teach away from their combination. See M.P.E.P. § 2145(X)(D)(2). In this case, Micron teaches away from complete interchangeability of memories.

Since it is improper to combine Intel with EN to show obviousness, since Fung does not disclose a power up detection circuit, nor do any of the references teach the use of burst EDO mode memory in combination with the other claimed elements, and since any combination of the disclosed concepts would therefore be inoperative, and since Micron teaches away from the use of interchangeable memory, the Appellant respectfully requests reconsideration and withdrawal of the rejection of claims 27-39 and 41-49 under 35 U.S.C. §103.

c.3 Why the claims are separately patentable:

While the separate patentability of each claim has been discussed in the "argument" section above, as allowed in the M.P.E.P. § 1206, the reasons are summarized here to ensure completeness and as a matter of convenience for the Board. Independent claim 26 includes a memory device operable with interchangeable burst EDO and fast page modes, and this

combination of elements is not included in the other independent claims. Neither EN, Intel, Fung, Farrer, Micron, nor Wyland disclose this combination of elements. Dependent claim 27 adds a power up detection circuit, responsive to a signal from the power supply, to cause the processor to detect the memory device mode and program the memory controller in accordance with the memory device mode. No proper combination of EN, Intel, Fung, Farrer, Micron, or Wyland disclose this element, in addition to the elements of the related independent claim. Independent claim 28 includes a power up detection circuit responsive to a signal from the power supply, to cause the processor to detect the memory device mode and program the memory controller. No proper combination of EN, Intel, Fung, Farrer, Micron, or Wyland disclose this element, in addition to the elements of the related independent claim.

Independent claim 29 includes a memory device having interchangeable burst EDO and EDO modes, and this combination of elements is not included in the other independent claims. Neither EN, Intel, Fung, Farrer, Micron, nor Wyland disclose this combination of elements. Dependent claim 30 adds a power up detection circuit, responsive to a signal from the power supply, to cause the processor to detect the memory device mode and program the memory controller in accordance with the memory device mode. No proper combination of EN, Intel, Fung, Farrer, Micron, or Wyland disclose this element, in addition to the elements of the related independent claim. Independent claim 31 includes a power up detection circuit responsive to a signal from the power supply, to cause the processor to detect the memory device mode and program the memory controller. No proper combination of EN, Intel, Fung, Farrer, Micron, or Wyland disclose this element, in addition to the elements of the related independent claim.

Independent claim 32 includes a memory device operable in a mode selected from burst EDO and a second mode, and variable timing of access control signals, and this combination of elements is not included in the other independent claims. No combination of EN, Intel, Fung, Farrer, Micron, or Wyland disclose this combination of elements. Dependent claim 33 adds a power up detection circuit, responsive to a signal from the power supply, to cause the processor to detect the memory device mode and program the memory controller in accordance with the memory device mode. No proper combination of EN, Intel, Fung, Farrer, Micron, or Wyland disclose this element, in addition to the elements of the related independent claim. Independent

claim 34 includes a power up detection circuit responsive to a signal from the power supply, to cause the processor to detect the memory device mode and program the memory controller. No proper combination of EN, Intel, Fung, Farrer, Micron, or Wyland disclose this element, in addition to the elements of the related independent claim.

Independent claim 35 includes a memory controller and a memory having two banks, one with burst EDO memory, and the second consisting of memory selected from EDO and fast page memory, and this combination of elements is not included in the other independent claims. No combination of EN, Intel, Fung, Farrer, Micron, or Wyland disclose this combination of elements. Dependent claim 36 makes the second bank memory type interchangeable. No proper combination of EN, Intel, Fung, Farrer, Micron, or Wyland disclose this element, in addition to the elements of the related independent claim. Independent claim 37 also has two banks, but each bank is independently interchangeable between burst EDO and a second type of memory. No proper combination of EN, Intel, Fung, Farrer, Micron, or Wyland disclose this element, in addition to the elements of the related independent claim.

Independent claim 38 includes a memory controller and a memory having two banks, one with burst EDO memory, and the second consisting of memory selected from EDO and fast page memory. In this case, access control signals are driven in response to information obtained from the banks, and this combination of elements is not included in the other independent claims. No combination of EN, Intel, Fung, Farrer, Micron, or Wyland disclose this combination of elements. Independent claim 39 also has two banks, but each bank is independently interchangeable between burst EDO and a second type of memory, and this combination of elements is not included in the other independent claims. No combination of EN, Intel, Fung, Farrer, Micron, or Wyland disclose this combination of elements.

Independent claim 40 includes a memory device selectively operable in burst EDO and second modes, and this combination of elements is not included in the other independent claims. No combination of EN, Intel, Fung, Farrer, Micron, or Wyland disclose this combination of elements. Dependent claim 41 adds a power up detection circuit, responsive to a signal from the power supply, to cause the processor to detect the memory device mode and program the memory controller in accordance with the memory device mode. No proper combination of EN, Intel,

Fung, Farrer, Micron, or Wyland disclose this element, in addition to the elements of the related independent claim. Independent claim 42 includes a power up detection circuit responsive to a signal from the power supply, to cause the processor to detect the memory device mode and program the memory controller. No proper combination of EN, Intel, Fung, Farrer, Micron, or Wyland disclose this element, in addition to the elements of the related independent claim.

Independent claim 43 does not claim the memory controller coupled to the bus, but does claim coupling the controller to the processor. This is true for claims 44-49 also. Dependent claim 44 adds the power up detection circuit acting to cause the processor to detect first and second modes of operation. Independent claim 45 has interchangeable burst EDO and a second type of memory. Dependent claim 46 adds the power up detection circuit acting to cause the processor to detect first and second sets of requirements. Independent claim 47 includes access control signals driven in response to information obtained from the first and second banks. Dependent claim 48 includes the power up detection circuit acting responsively to a signal from the power supply to program the memory controller. Independent claim 49 includes the power up detection circuit acting responsively to a signal from the power supply, so as to cause the processor to detect sets of requirements, and to program the memory controller in accordance with the requirements. None of these limitations depends on the other, and each dependent claim is separately patentable from the other, as well as from the independent claims.

9. SUMMARY

It is respectfully submitted that the art cited does not anticipate the claimed invention, nor does the cited art render the claimed invention obvious. It is respectfully submitted that claims 26-49 should therefore be allowed. Reconsideration and withdrawal of the rejections of claims 26-49 is hereby respectfully requested. Should the Board be of the opinion that a rejected claim may be allowable in amended form, an explicit statement to that effect is also respectfully requested.

CONCLUSION

The Appellant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone the Appellant's attorney Mark Muller at (210) 308-5677, or the undersigned to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 10th day of December, 2002.

Name Amy Moriarty

Signature Amy Moriarty